~~can be used to implement massively parallel digital-to-analog conversion.~~ ~~Parallel~~ Such parallel digital-to-analog conversion is useful in many applications such as digital communications, image display, and shared parallel analog-to-digital conversion ~~where it is desired to convert multiple digital numbers to analog signals.~~

B1 end

In the Claims:

Claim **4** has been amended as follows:

4. (Amended) The machine of claim **3** in which said first digital clock is a variable-frequency digital clock, ~~has a frequency that can vary,~~ whereby said first count need not always change at a single rate, whereby high-precision digital-to-analog conversion is possible with a high frequency of said first digital clock, a high rate of change of said first count, and a corresponding high dynamic power consumption and low-precision digital-to-analog conversion is possible with a low frequency of said first digital clock, a low rate of change of said first count, and a corresponding low power dynamic power consumption ~~the machine of claim 1 can be used for digital-to-analog conversion of varying precision without the need for said first counter to always change at the fastest possible rate~~.

B2

GENERAL REMARKS

The Notice of Non-Compliant Amendment Letter of May 22, 2003 requested a marked-up version of the replacement paragraph (namely the amended Abstract) in the specification and a marked-up version of the amended claim (namely claim **4**).

Above the Applicant has provided a marked-up version of the amended Abstract and a marked-up version of amended claim **4**. In the marked-up material, deletions are indicated with a strike-through text format, and additions are indicated with an underlined text format, per the reference Sample Amendment Format included with the Notice of Non-Compliant Amendment letter. The Applicant incorporates Amendment A by reference, and provides the above marked-up material as an addendum to meet the